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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/071,379
Filing Date: February 06, 2002
Appellants: BOBBA ET AL.

Mr. Wasif Qureshi
For Appellants

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08 August 2005

(1) Real Party in Interest

A statement identifying the real party of interest as Sun Microsystems, Inc. is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct. Claims 1 and 3 – 15 are pending and stand rejected in this application. Appellants have canceled claim 2.

(4) Status of Amendments

Appellants' statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1 and 3 – 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,596,506 to Petschauer et al. (hereinafter, "Petschauer"), in view

of U.S. Patent No. 6,285,208 to Ohkubo. This rejection is set forth in a prior Office Action, mailed on 07 September 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

1. Claims 1 and 3 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,596,506 to Petschauer et al (hereinafter, "Petschauer") in view of U.S. Patent No. 6,285,208 to Ohkubo.

2. Referring to claim 1, Petschauer discloses an integrated circuit that includes (a) a signal driver that generates a signal on a signal path (Fig. 1; column 6, lines 10 – 29); (b) a wire disposed adjacent to the signal path (column 6, lines 47 – 58); and (c) circuitry that generates a value on the first wire (a "0" to "1" transition) that causes a discharge of capacitance between the signal path and the first wire (column 8, lines 10 – 18). Petschauer's invention pertains to crosstalk and noise minimization and prevention techniques in complex IC designs (column 1, lines 34 – 65), and this is basically the main reason why shielding is performed in circuit designs. However, Petschauer does not teach the use of shield control circuitry. Ohkubo on the other hand, teaches a semiconductor IC that includes signal lines, a plurality of shield wiring lines,

as well as shield control circuitry (see Figs. 5; 10 and 11), and discloses how effective shielding in IC circuits can be accomplished using his shielding methodology. Thus, Petchauer and Ohkubo disclose all the elements of claim 1. As per claim 3, see Petschauer - Figs. 3A and 3B which show the capacitor, as claimed. As per claims 4 and 5, see Petschauer - Figs. 1, 10A and 10B, which show the driver as a gate and as transistors, as claimed. Petschauer does not teach the limitations of claims 6 – 12 and15, however Ohkubo discloses all the claimed elements. Referring to claim 6, see Ohkubo, Fig. 11, which shows the shield control circuitry (W12, W22, etc) dependent on the signal driver as claimed. As for claim 7, see Ohkubo, Fig. 5, which shows the two wires (S1 and S2) are used to shield the signal wire (F2) as claimed. Regarding claims 8 and 9, see Ohkubo - Fig. 10; column 8, line 60 to column 9, line 5, which shows the use of synchronous and asynchronous signals as claimed. As for claims 10 and 11, see Ohkubo – Fig. 10 (blocks W11, W21, etc) that shows a shield control circuitry that includes a delay element (in this case, a NOR gate which can be used as a delay element) as well as an inverter, as claimed. The inclusion of that gate guarantees that the delay will be greater than the signal propagation delay of the signal, as claimed in claim 11. As per claim 12, see Ohkubo - Figs. 5, 6F, 6G and 6H, which show how the wires shielding the signal path are controlled to only participate in discharge events ("0" to "1" transitions) as claimed. Referring to claim 13, see Petschauer column 11, lines 3 – 36, which teach how the charging and discharging of the capacitor takes place when the signal transitions from "0" to "1", and "1" to "0" as claimed. Claim 14 has the same limitations as claim 3, and so the same rejections apply. As per claim 15, see Ohkubo,

Fig. 10, which shows how to selectively delay the driving of the wire to a second potential by controlling the inputs IN1, IN2, IN3, etc, as claimed. Since the use of shielding and shielding control has become an essential feature in complex high speed IC designs in order to eliminate or minimize crosstalk and noise problems created by cross-coupling capacitances, it would therefore be obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Petschauer and Ohbuto to achieve the same inventions as claimed.

(7) Response to Argument

A. *Claims 1 and 3 – 15 are Unpatentable over Petschauer and Ohkubo under 35 U.S.C. 103(a)*

1. Petschauer and Ohkubo Disclose all the Limitations of Claims 1 and 3 – 11

Appellants assert that the prior art references of Petschauer and Ohkubo whether considered separately or in any combination do not establish a *prima facie* case of obviousness since they do not suggest or teach *all* of the claimed elements of the invention (see Appellants' brief, pages 8 – 9). The Examiner respectfully disagrees. Turning first to Appellants' independent claim 1, Appellants correctly state that claim 1 requires:

> Shield control circuitry that after a transition on the signal path, causes the first wire to transition to a value that causes a charge up of capacitance between the signal path and the first wire, wherein a subsequent transition on the signal path causes a discharge of capacitance between the signal path and the first wire.

Appellants' Brief, page 9. Figure 3a, shown below, illustrates Appellants' shield control circuitry.

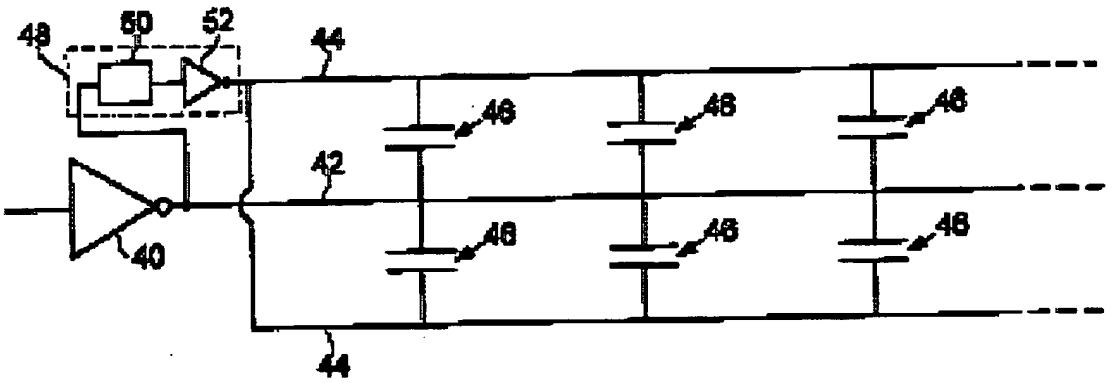
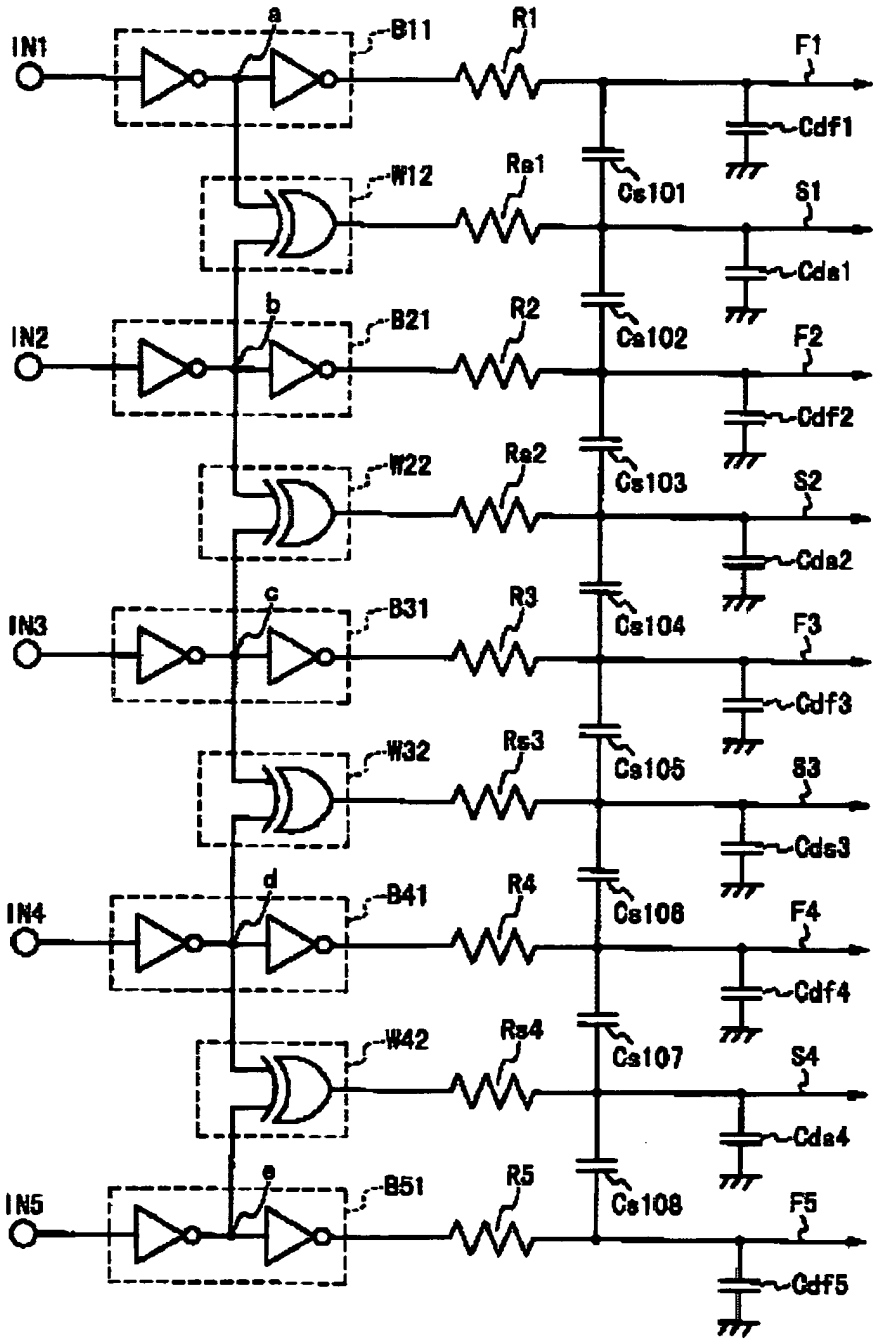


FIGURE 3a

The Appellants concur with the Examiner's assertion that Petschauer fails to disclose the use of shield control circuitry. Appellants rely on Ohkubo's Figure 5 to support their arguments that Ohkubo does not teach the capacitive charge and discharge sequences and transitions as required by claim 1 (Appellants' Brief – page 10). Examiner however relies on Ohkubo's Figure 11, which discloses shield control circuitry, and the sequence of capacitive charging and discharging disclosed by Ohkubo satisfy requirements of Appellants' claim.

Fig. 11


IN1
IN2
IN3
IN4
IN5
a
b
c
d
e
B11
B21
B31
B41
B51
W12
W22
W32
W42
R1
R2
R3
R4
R5
Rs1
Rs2
Rs3
Rs4
Cs101
Cs102
Cs103
Cs104
Cs105
Cs106
Cs107
Cs108
F1
F2
F3
F4
F5
S1
S2
S3
S4
Cdf1
Cdf2
Cdf3
Cdf4
Cdf5
Cds1
Cds2
Cds3
Cds4

Referring now in detail to Ohkubo - Fig. 11, *supra*, Ohkubo discloses an input signal ***(for the purpose of this analysis, we will consider the input signal labeled IN3***), applied to an inverting driver, whose output is labeled "c"; whereas the output of that inverting driver is applied to: (1) another inverter whose output is connected to the signal wire labeled F3 (both inverters are in a block ***labeled "B31"***); and (2) two non-inverting XOR gates labeled W22 and W32, connected to a first adjacent wire shield labeled S2 and a second adjacent wire shield labeled S3.

Fig. 11 illustrates the signal F3 (which includes two inverters connected in series shown in ***Block 31***). F3 is logically inverted with respect to the shield signals S2 and S3, since both S2 and S3 paths include an inverter and an XOR (non-inverting) gate connected in series. It is well known in the art of integrated circuit design that an XOR gate intrinsically and inherently has a larger gate delay than an inverter. Thus the XOR gates W22 and W32 are similar to the Appellants' delay element labeled 50 shown in the Appellants' Figure 3a, *supra*, since in Ohkubo these XOR gates introduce a larger path delay in the two wire shield paths S2 and S3 than in the signal wire path F3 just as the delay element 50 in Figure 3a introduces more delay in the shield paths 44. Thus, Ohkubo's Figure 11, *supra,* is structurally equivalent to Appellants' Figure 3a, *supra.* Appellants' Figure 3a and Appellants' specification paragraphs 0025 – 0028 disclose the sequence of charging and discharging of capacitance.

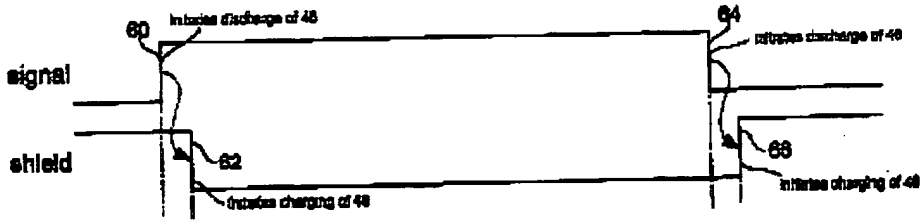


FIGURE 3b

Per the Examiner's arguments, *supra*, since Ohkubo's circuit is structurally equivalent to Appellants' circuit, the sequence of charging and discharging of the capacitances shown by Appellants in Figure 3b, *supra*, and described in Appellants' specification paragraphs 0025 – 0028 also applies to Ohkubo's circuit. Accordingly, Appellants' assertion (Appellants' Brief, pages 9 and 10) that Ohkubo clearly shows a value of a shield wire that is controlled to transition with a transition of a signal shielded by a shield wire, and not after a transition of a signal as require by independent claim 1 is ***clearly incorrect***.

As explained above, Ohkubo's Figure 11 shows a signal F3 that is inverted with respect to the two adjacent shield wires S2 and S3. Furthermore, since the non-inverting XOR gates (whose outputs W22 and W32 drive the shield wires S2 and S3) have a larger gate delay than the inverter whose output drives the signal wire F3, it therefore follows that Ohkubo's Figure 11 circuit, *supra*, teaches the Appellants' claim that the value of the shield wires (S2 and S3) is controlled to transition ***after*** **a transition of a signal F3 shielded by the shield wires S2 and S3**, as required by

independent claim 1, and ***not*** **with a transition**, as asserted by Appellants' (Appellants' Brief, page 10).

In summary, Ohkubo's Figure 11, *supra,* discloses a ***signal driver that generates a signal*** on a signal path (Block B31); a first ***wire disposed adjacent to the path*** (S2 or S3); ***and shield control circuitry*** (Block W22 or W32) that, ***after a transition*** on the signal path, causes the first wire to transition to a value that causes a ***charge up of capacitance*** between the signal path and the first wire (capacitors Cs104 or Cs105), wherein a ***subsequent transition*** on the signal path causes a ***discharge of capacitance between the signal path*** and the wire.

The Examiner therefore respectfully maintains that the circuit shown in Ohkubo - Fig. 11, *supra,* teaches, or at the very least, suggests, all the limitations claimed of claim 1 and all claims dependent therefrom.

2. Petschauer and Ohkubo Disclose all the Limitations of Claim 12

Turning next to Appellants claim 12, Appellants correctly state that this claim refers in part to:

> driving means for generating a signal on a signal path; and
> shielding control for actively controlling a value on wires shielding that signal path such that the driving means only participates in discharge events.

Appellants argue that the prior art cited by the Examiner does not teach the elements of claim 12 pertaining to wires shielding a signal path participating ***only in discharge events*** (Appellants' Brief, pages 11 and 12). According to the Appellants, this is because the signals created between the signal path and the shield wire signals

are logically inverted and delayed with respect to each other as stated above. However, as cited in ***section1 supra,*** Ohkubo indeed discloses a circuit, see Fig. 11, *supra,* which ***contains a logic inversion and delay*** between the signal path F3 and the shielding wires W22 and W32, causing the cross-coupling capacitors Cs104 and Cs105 to ***participate only in discharge events***, as claimed. Although Appellants argue that their invention depends on driving the shield wire to a phase opposite to that of the signal, Appellants' claim language does not address the limitation of signal phases. As stated above, and also by Petschauer (see col. 1, line 43 – col. 2, line 2; col. 8, line 10 - 20), it is very well known in the art that crosstalk and noise injected in circuits are caused by the charging and discharging of cross-coupling capacitors, and therefore controlling the charging and discharging sequence in neighboring wires can significantly reduce circuit crosstalk and noise.

Therefore, Petschauer and Ohkubo in combination disclose, or at the very least suggest, all the claimed limitations of claim 12.

3. Petschauer and Ohkubo Disclose all the Limitations of Claims 13 – 15

Regarding independent claim 13, Appellants correctly state that the claim in part includes the limitations of:

> after the signal on the signal path has transitioned to a first voltage potential, charging a capacitor by causing a wire to transition to a second voltage potential, wherein the wire shields the signal path; and discharging the capacitor when the signal path transitions to the second voltage potential.

Appellants again argue (Appellants Brief, pages 12 and 13) that Ohkubo fails to disclose charging up a capacitance between a signal and a shield wire ***after a***

transition on the signal, and thus there is no charging of a capacitor in Ohkubo, and that Ohkubo necessarily fails to disclose discharging the capacitor when the signal subsequently transitions as required by independent claim 13. However, as indicated in Figure 11 and section 2, *supra*, the logic inversion between the signal wire (F3) and the shields (S2 and S3), as well as the gate delay difference between an inverter and an XOR gate cause the capacitor between the signal wire and shields to charge and discharge in a sequence similar to the Appellants' claimed sequence. Furthermore, claims 14 and 15 are dependant upon claim 13, and are obvious under 35 U.S.C. § 103(a) for the reasons cited above.

Therefore, Petschauer and Ohkubo in combination disclose, or at the very least suggest, all the claimed limitations of independent claim 13 and it's dependent claims 14 and 15.

4. Motivation for Combining Petschauer and Ohkubo is Provided

Appellants maintain that the Examiner has not provided a motivation or suggestion to combine both inventions in order to obtain the same claimed invention. However, as stated *supra*, ***crosstalk and noise injection*** due to cross-coupling capacitances in complex, high-performance IC designs are ***a major concern***, and methods of ***reducing*** or ***eliminating crosstalk*** and noise injection are of ***paramount importance*** in the art. Ohkubo teaches that ***signal wires*** used to connect circuit blocks in an integrated circuit are always ***accompanied by parasitic capacitances***. Ohkubo recites that ***large parasitic*** capacitances can ***slow down the circuit*** operating speed of the circuit and can ***also increase crosstalk*** and noise injection in the circuit, resulting in

an ***increase in chip size*** and a ***decrease in production yield***. Therefore, Petschauer and Ohkubo are considered to be ***analogous art***. Petschauer teaches a method of fabricating an integrated circuit, and discloses how the ***crosstalk voltages*** caused by the ***charging and discharging*** of the cross-coupling capacitances in IC designs can be ***estimated*** and ***subsequently reduced*** through ***layout techniques***, while Ohkubo cites means of ***effectively shielding*** a signal wire in a semiconductor integrated circuit by using ***adjacent shielding wires and control circuitry***, as discussed in detail, *supra*. Once again, as noted *supra*, Ohkubo's Figure 11 shows the circuit, which provides the ***same claimed charge/discharge events*** and ***sequence for effectively shielding*** a signal wire. The Examiner therefore strongly believes that he has established a *prima facie* case of ***obviousness and motivation*** so that a person of ordinary skill in the art at the time of the invention is able to ***combine*** Ohkubo and Petschauer to ***achieve the same claimed limitations***.

Having ***carefully considered all*** of Appellants' arguments, the Examiner maintains that the Petschauer and Ohkubo references in combination at the very least suggest, if not disclose, the argued limitations of Appellants' invention. Accordingly, based on the foregoing, the Examiner respectfully requests the rejections of claims 1 and 3 – 15 under U.S.C. § 103(a) as ***unpatentable*** over Petschauer in view of Ohkubo be ***affirmed***.

(8) Claims Appendix

The claims involved in the Appeal cited by Appellants in Claims Appendix are correct.

(9) Evidence Appendix

Appellants' statement in the Evidence Appendix is correct.

(10) Related Proceedings Appendix

Appellants' statement in the Related Proceedings Appendix is correct.

Respectfully submitted

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MYD

05 October 2005

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